CBCS SCHEME

USN | | | | | | | | | | |

18EC62

Sixth Semester B.E. Degree Examination, June/July 2023
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. List the different registers of ARM CORTEX-M3 and mention their use. Explain the use of link register with an illustration. **(08 Marks)**

b. Explain Program Status Register (PSR) configuration. Illustrate how to access different subdivisions of PSR. **(06 Marks)**

c. Explain exceptions and interrupts of ARM CORTEX-M3. **(06 Marks)**

OR

2 a. Explain the operation modes of CORTEX-M3 with a block diagram. **(08 Marks)**

b. Explain CORTEX-M3 stack implementation for push and pop operations. **(06 Marks)**

c. Explain reset sequence of CORTEX-M3 why LSB of reset vector address is set to 1. **(06 Marks)**

Module-2

3 a. Explain following instruction of ARM CORTEX-M3 with suitable illustration:
(i) BIC (ii) SBFX (iii) REVSH (iv) LDRH **(08 Marks)**

b. Write an assembly language program to find sum of all even numbers in a given array of 10 numbers. **(06 Marks)**

c. Explain conditional execution using IT instructions with an example. **(06 Marks)**

OR

4 a. Explain all shift and rotate instructions of CORTEX-M3 with illustration. How rotate left operation can be implemented? **(10 Marks)**

b. Write an assembly language program to determine the parity of a 32 bit number. If even parity store 00h in a memory location otherwise store FFh in the location. **(06 Marks)**

c. Assume R0 = 0X12345678, R1 =0XFEDCBA12. Write the result after executing following instructions:
(i) BFC.W R0, #8, #16
(ii) UBFX.W R0, R1, #4, #8
(iii) BFI.W R1, R0, #8, #16
(iv) REVSH R1, R0 **(04 Marks)**

Module-3

5 a. Explain Big Endian and little Endian operation and give examples. **(06 Marks)**

b. With a diagram, explain SRAM cell implementation and its working. Give comparison between SRAM and DRAM cells. **(08 Marks)**

c. Explain the sequence of operation for communicating with an I2C slave device. **(06 Marks)**

OR

6 a. Give comparison between RISC and CISC. **(06 Marks)**

b. With a circuit diagram, explain how input and output circuits of a processor can be isolated. **(06 Marks)**

c. Explain SPI Bus interfacing and sequence of operation for communicating with a SPI device. **(08 Marks)**

Module-4

7 a. Explain characteristics of an embedded system with examples for each. **(06 Marks)**

b. Explain state machine model (FSM) by considering automatic seat belt warning system. **(08 Marks)**

c. Discuss advantages and drawbacks of super loop based firmware design approach. **(06 Marks)**

OR

8 a. Explain any six nonoperational quality attributes. Explain product life cycle curve. **(10 Marks)**

b. Design an automatic tea/coffee vending machine based on FSM model for the following requirement:
The tea/coffee vending is initiated by user inserting a 5 rupees coin. After inserting coin, the user can either select 'Coffee' or 'Tea' or press 'Cancel' the order and take back the coin. **(06 Marks)**

c. Explain the assembly language to machine language conversion process with block diagram. **(04 Marks)**

Module-5

9 a. Explain monolithic and micro kernels with suitable example for each. **(06 Marks)**

b. Explain task, process and threads. **(08 Marks)**

c. Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 ms respectively enter the ready queue together in order P1, P2, P3. Calculate waiting time and turn around time for each process and average waiting time and TAT. (Assume there is no I/O waiting for the processes) **(06 Marks)**

OR

10 a. Explain different conditions that favour deadlock. Explain techniques to detect and prevent deadlock. **(08 Marks)**

b. With a block diagram, explain the concept of counting semaphore. Give real world example. **(08 Marks)**

c. Explain the advantages of simulation based debugging. **(04 Marks)**

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